UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,562	09/23/2003	Jose A. Tierno	YOR920030375US1	3065

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EXAMINER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _17 July 2008_.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-23_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-23_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _23 September 2003_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicants' arguments filed on 07/17/2008 have been fully considered but they are not persuasive.

Applicant's Argument: Applicants argue that "Yada reference fails to teach or suggest "generating at least one sampling from the received input signal based on <u>a clock signal unrelated to a clock signal used to recover data associated with the received input signal</u>.""

Examiner's Response: Examiner respectfully disagrees. Examiner asserts that as disclosed by Yada a sampling clock of frequency F_s, is supplied to ADC 4 to sample the input signal. Yada further discloses that the data detector 6 (interpreted as the recovery circuit) is supplied with a clock signal generated by a PLL circuit 7 (see column 8, last paragraph). Although, in column 8, lines 65-68, Yada discloses that PLL extracts a clock signal from the waveform equalized digitized audio signal, <u>Yada does not indicate that the extracted clock is the clock used by ADC 4</u>. Yada specifically states extracting <u>a</u> (and not <u>the</u>) clock signal from the waveform equalized digitized audio signal. Therefore the clock used by ADC 4 is not the clock used by data detector 6.

Applicant's Argument: Applicants argue that "the Examiner fails to identify a cogent motivation for combining Ariyavisitakul and Yada."

Examiner's Response: Examiner respectfully disagrees. Examiner asserts that, as cited in the last office action, it would have been obvious to one of ordinary skill in the art at the time of invention to use a clock for sampling the received

signal unrelated to the clock used for data recovery purposes to make the

process of data recovery faster. If the clocks are the same, data recovery circuit

needs to extract the clock from the incoming signal before processing the signal.

This process is time consuming. However, if the data recovery circuit has its own

local clock, there is no need for extracting the clock and the incoming signal can

be processed immediately by using the local clock. Reducing the time required

for signal processing (here the data recovery process) is always desirable in

communication systems and the teachings of Yada helps to reduce the

processing time of the signal in the apparatus disclosed by Ariyavisitakul.

Applicant's Argument: Applicants argue that "Ariyavisitakul does not contain

the disclosure which is necessary to support a rejection of claim on the basis of

inherency."

Examiner's Response: Examiner respectfully disagrees. As discussed in the

last office action, Ariyavisitakul discloses generating at least one sampling from

the received input signal (see block 104 and column 10, last paragraph). Since

every sampling device known in the art needs to have a clock in order to function

properly (sample the signal), therefore it is a valid statement to say that sampling

device 104 inherently has a sampling clock.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for

all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2.   Claims 1, 3, 9-11, 13, and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ariyavisitakul et al. (hereafter, referred as Ariyavisitakul) (US 5,222,101), in view of Yada et al. (hereafter, referred as Yada) (US 5,260,836).

As to claim 1, Ariyavisitakul discloses a method of equalizing (see Fig. 1 and column 1, last paragraph) an input signal 101 received from a communication channel, comprising the steps of: generating at least one sampling from the received input signal based on a clock signal (see block 104 and column 10 last paragraph) (i.e. inherently by using a clock signal); and compensating for distortion associated with the communications channel based on at least a portion of the at least one generated sampling (see the abstract, lines 3-5). Ariyavisitakul discloses all the subject matters claimed in claim 1, except that the sampling clock is not related to the clock signal used to recover data associated with the received input signal. Yada, in the same field of endeavor, shows a system (see Figs. 1A and 1B) comprising a sampling device 4, an equalizer 5, a data detector 6, and a PLL circuit 7. Yada discloses that a sampling clock of frequency F_s, is supplied to ADC 4 to sample the input signal. Yada further discloses that the data detector 6 (interpreted as the recovery circuit) is supplied with a clock signal generated by a PLL circuit 7 (see column 8, last paragraph). Therefore Yada teaches that the sampling clock is not related to the clock signal used to recover data associated with the received input signal. It would have been obvious to one of ordinary skill in the art at the time of invention

to use a clock for sampling the received signal unrelated to the clock used for

data recovery purposes to make the process of data recovery faster (i.e. without

spending time on recovering the clock of the transmitter and by using receiver's

local clock).

As to claim 11, Ariyavisitakul discloses an apparatus (see Fig. 1) for

equalizing an input signal 101 received from a communication channel (see

column 10, last paragraph), comprising: a memory 105; and at least one

processor coupled to the memory and operative to: (i) generate at least one

sampling from the received input signal (see block 104 and column 10 last

paragraph) (i.e. inherently by using a clock signal); and (ii) compensate for

distortion associated with the communications channel based on at least a

portion of the at least one generated sampling (see the abstract, lines 3-5).

Ariyavisitakul discloses all the subject matters claimed in claim 11, except that

the sampling clock is not related to the clock signal used to recover data

associated with the received input signal. Yada, in the same field of endeavor,

shows a system (see Figs. 1A and 1B) comprising a sampling device 4, an

equalizer 5, a data detector 6, and a PLL circuit 7. Yada discloses that a

sampling clock of frequency F_s, is supplied to ADC 4 to sample the input signal.

Yada further discloses that the data detector 6 (interpreted as the recovery

circuit) is supplied with a clock signal generated by a PLL circuit 7 (see column 8,

last paragraph). Therefore Yada teaches that the sampling clock is not related to

the clock signal used to recover data associated with the received input signal. It

would have been obvious to one of ordinary skill in the art at the time of invention

to use a clock for sampling the received signal unrelated to the clock used for

data recovery purposes to make the process of data recovery faster (i.e. without

spending time on recovering the clock of the transmitter and by using receiver's

local clock).

As to claims 3 and 13, Ariyavisitakul further discloses that the distortion

compensating further comprises: setting one or more parameter values based on

the at least a portion of the at least one generated sampling (see Fig. 1, block

106, column 10, last paragraph and column 9, lines 33-35); and applying the one

or more parameter values to the received input signal (see column 9, lines 35-

38).

As to claims 9 and 19, Ariyavisitakul discloses that the communication

channel is a digital communications channel (see the abstract and column 1,

second paragraph).

As to claims 10 and 20, Ariyavisitakul discloses that the equalization is

performed in accordance with a data receiver coupled to the communications

channel (see column 10, last paragraph and the abstract).

As to claim 21, Ariyavisitakul discloses an equalization system responsive

to an input signal received from a communication channel (see Fig. 1),

comprising: a sampling module, the sampling module 104 (see column 10, last

paragraph) generating at least one sampling from the received input signal (i.e.

inherently by using a clock signal); and a filter (equalizer 107), the filter

compensating for distortion associated with the communication channel based

(see the abstract and column 10, last paragraph and column 1, lines 33-38) on

an equalization algorithm which is responsive to at least a portion of the at least

one sampling generated by the sampling module (see the abstract, lines 3-5).

Ariyavisitakul discloses all the subject matters claimed in claim 21, except that

the sampling clock is not related to the clock signal used to recover data

associated with the received input signal. Yada, in the same field of endeavor,

shows a system (see Figs. 1A and 1B) comprising a sampling device 4, an

equalizer 5, a data detector 6, and a PLL circuit 7. Yada discloses that a

sampling clock of frequency F_s, is supplied to ADC 4 to sample the input signal.

Yada further discloses that the data detector 6 (interpreted as the recovery

circuit) is supplied with a clock signal generated by a PLL circuit 7 (see column 8,

last paragraph). Therefore Yada teaches that the sampling clock is not related to

the clock signal used to recover data associated with the received input signal. It

would have been obvious to one of ordinary skill in the art at the time of invention

to use a clock for sampling the received signal unrelated to the clock used for

data recovery purposes to make the process of data recovery faster (i.e. without

spending time on recovering the clock of the transmitter and by using receiver's

local clock).

As to claim 22, Ariyavisitakul further shows that the equalization system is

part of a data receiver (see Fig. 1).

As to claim 23, Yada discloses that the equalization system 5 is

independent of a clock and data recovery system 6 of the data receiver (see

Figs. 1A and 1B).

3.   Claims 2 and 12 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Ariyavisitakul and Yada, further in view of Hsu et al. (hereafter,

referred as Hsu) (US 2004/0062329).

As to claims 2 and 12, Ariyavisitakul discloses that demodulator 104

oversamples the IF signal at a multiple of the symbol rate since optimum time for

sampling the signal is unknown. Ariyavisitakul and Yada are silent in disclosing

that the sampling (oversampling) generation step comprises the steps of:

generating multiple phases of the sampling clock signal; and sampling the

received input signal at the respective multiple phases of the sampling clock

signal to generate respective multiple samples. Hsu, in the same field of

endeavor, discloses an apparatus (see Fig. 1) comprising an oversampler 24 that

samples the data using multiple clocks 26, producing 4 sampled signals. Hsu

further discloses that the clocks are generated by a VCO 30 and are clocks of the

same frequency and four different phases (see paragraph 0003). It would have

been obvious to one of ordinary skill in the art at the time of invention to use

multiple phases of a sampling clock to sample the input signal and determine the

optimum clock for sampling the incoming data (see paragraph 0003) as

suggested by Hsu.

4.   Claims 4 and 14 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Ariyavisitakul and Yada, further in view of Dally et al.

(hereafter, referred as Dally) (US 2003/0086339).

As to claims 4 and 14, Ariyavisitakul and Yada are silent in disclosing that

the sampling clock signal has a lower frequency than the data recovery clock

signal. Dally, in the same field of endeavor, discloses a clock recovery circuit

wherein the sample clock is slower (interpreted as having lower frequency) than

the data clock (see paragraph 0060). It would have been obvious to one of

ordinary skill in the art at the time of invention to make the sample clock slower

than the data clock to maintain the synchronization between two clocks (data

clock and sample clock) as suggested by Dally (see paragraph 0061) and recover

the data.

5.   Claims 5, 6, 8, 15, 16, and 18 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Ariyavisitakul and Yada, further in view of Shattil (US

2004/0243258).

        As to claims 5 and 15, Ariyavisitakul and Yada disclose all the subject

matters claimed in claims 1 and 11, except for validating the at least one

generated sampling. Shattil discloses a receiver (see Fig. 10) comprising: a

sampler 1002 to provide samples to selector 1004, wherein the selector provides

weights to the samples (interpreted as validating the samples) (see paragraph

0124). It would have been obvious to one of ordinary skill in the art at the time of

invention to modify Ariyavisitakul and Yada as suggested by Shattil to select only

samples which their power levels meet a predetermined threshold to enhance the

integrity of the output signal.

        As to claims 6 and 16, Shattil further discloses comparing samples of the

at least one generated sampling to a validation threshold (see paragraph 0124).

It would have been obvious to one of ordinary skill in the art at the time of

invention to modify Ariyavisitakul and Yada as suggested by Shattil to select only

samples which their power levels meet a predetermined threshold to enhance the integrity of the output signal.

As to claims 8 and 18, Shattil further discloses discarding samples of the at least one generated sampling that are determined to be invalid (see paragraph 0124). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Ariyavisitakul and Yada as suggested by Shattil to enhance the integrity of the output signal.

6.   Claims 7 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ariyavisitakul, Yada, and Shattil, further in view of Best et al. (hereafter, referred as Best) (US 6,570,944).

As to claims 7 and 17, Ariyavisitakul, Yada, and Shattil disclose all the subject matters claimed in claims 5 and 15, except for generating leading edge samples and trailing edge samples from the received input signal; and varying an eye center threshold to determine the validity of the at least one generated sampling. Best, in the same field of endeavor, disclose an apparatus that reduces sampling errors for data communicated between devices (see the abstract). Best disclose that in any high-speed signaling system, the ability of the receiving device to sample the data signal at a precise instant within the valid data interval (the "data eye") is often a critical factor in determining how brief the data eye may be. Best further discloses that any technique for more accurately controlling the sampling instant within the data eye generally permits faster data transfer and therefore higher signaling bandwidth. Best further shows generating leading edge samples and trailing edge samples from the received input signal

(see Fig. 2) and delaying the signal so that the delayed signal transitions at the midpoint of the data eye (interpreted as varying an eye center threshold to determine the validity of the at least one generated sampling). Therefore, for the reasons stated above, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Ariyavisitakul, Yada, and Shattil as suggested by Best.

Conclusion

7.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leila Malek whose telephone number is 571-272-8731. The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021.

The fax phone number for the organization where this application or proceeding

is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

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Representative or access to the automated information system, call 800-786-

9199 (IN USA OR CANADA) or 571-272-1000.

                                                    Leila Malek
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/L.M./
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